

Address (hex)	Register	Direction	Bits	PV (vht)	Function	CONSTANT VALUES	PLACE HOLDERS	PV record type	explained
0x0	SSD ID	ro	15-0	l	0x5344	0x5344	OK	m=msbindex (bimap)	
0x1	Board ID	ro	3-0	l	Board jumper		1 pins	address (trig) int	
0x2	FPGA build number	ro	15-0	l	build number	0x0001	OK	rs=rsbindex (bimap)	
0x3	SIU Data format version	ro	7-0	l		0x01	OK	rs=rsbindex (bimap)	
status									
0x10	Fiber link status	ro	7-0	m	current link status		4444 ?	rs=rsbindex (bimap)	do we have functionality at the moment? yes marcos
0x11	LC FPGA status	ro	15-8	m	link loss since last reset		OK		checking that 0x802 ... 0xF02 are 0x0110
0x12	Clear Status Latch	wo	7-0	b	indicate correct data pattern is received		Not Connected		
0x12	Clear Status Latch	wo	7-0	b	Clears the status latch		OK		
status counters									
0x30	Reset status counters	wo	0	b			OK		
0x31	TCD triggers received	ro	1	l			Implemented		Tests shows abnormal behaviour
0x32	TCD level 0 received	ro	1	l			OK		Counter of the TCD triggers read by data_packer
0x33	SIU packet counter	ro	1	l			OK		Counter of the words read by DLL
0x34	RHIC strobe LSB	ro	15-0	l*			OK		
0x35	RHIC strobe MSB	ro	15-0	l*			OK		
0x36	HOLD	ro	15-0	l	HOLDS generated		OK		
0x37	TEST	ro	15-0	l	TESTs generated		OK		
Pedestal pattern									
0x20	Loop count	rw	15-0		indirect read loop amount		FF20		
0x21	ADDR LSB	rw	15-0		indirect Addr LSB		FF21		
0x22	ADDR MSB	rw	15-0		indirect Addr MSB		FF22		
0x23	Data LSB	rw	15-0		indirect Data LSB		FF23		
0x24	Data MSB	rw	15-0		indirect Data MSB (increments addr)		FF24		
LVDS re calibration									
0x40	calibration_EN	RW	0	b	1=recalibration process for LVDS link 0=normal op				
DAQ									
0x80	Fiber Enable	rw	7-0	m	Bit pattern to enable fibers for DAQ		FFFF ?		All fibers produce header by default, is this the purpose?
0x81	Test2hold delay	rw	7-0	l	test to hold delay (in 25ns steps)		OK		
0x82	TCD delay	rw	7-0	l	delay between LD and hold (in 25ns steps)		OK		
0x83	Enable TCD triggers	rw	15-8	b	TCD enable each bit to each channel		OK		This Register may change in future versions
			7-4		forced triq mode 0		OK		This Register may change in future versions
			3-0		forced triq mode 1		OK		
0x84	Enabled triggers	wo	7-0		forced triq mode 0		OK		
			15-8		forced triq mode 1		OK		
0x85	Data format	rw	3-0	e	select triq mode	DIFFERENCE	OK		
			7-4	e	data format (raw, compressed, ...)		OK		
			7-4	e	minimum bias raw data rate		OK		
0x86	Reset data buffers	wo	0	b			Not Connected		
0x87	SIU Buffer status	ro	0	m			EEEE ?		Which is the SIU buffer? 32 k fifo data backer or 512 SUI fifo
Ladder card/Fiber 0 (CHANNEL)									
0x800	LC x FPGA confio control	wo	3-0		0 = no out of abort / 1 = do the reset sequence / 2 = ready to data / 3 = idle		OK		
0x801	LC x FPGA confio data	wo	15-0		Data written to DATA0 line		OK		
0x802	LC x FPGA confio status	ro	0	b	Abort flag		OK		
			4	b	LC_NSTATUS flag		OK		
			8	b	LC_NSTATUS		OK		
			15-12	e	confio_engine state: 0 = IDLE, 1 = PRESET, 2 = RESET, 3 = CONF_L, 4 = CONF_H, 5 = INIT, 6 = USER, 7 = ABORT (Refer to Cyclone III configuration datasheet to make sense of this states)		OK		
0x804	LC x JTAG control	wo	7-0		TDO data	Automatically put TDO into output buffer	OK		
			15-8		TAP state control word		OK		
0x805	LC x JTAG reset	wo	0		RSTB line to ladder card		OK		
			7-0		TDO data		OK		JTAG TDO sets written to readback fifo after each write to 0x804 NOTE this doesn't have a register
			15-8		TAP state control word		OK		
0x808	LC x ADC offset	rw	9-0	l	ADC base line shift		OK		
0x809	LC x ZS threshold	rw	9-0	l	Threshold		OK		
			12	b	pulse polarity (0=pos)		OK		
0x80A	L x Fiber status	ro	0		DES_Lock		DDO(CHANNEL) ?		Do we have the functionality for this? yes marcos
			1		Rx_Loss		OK		
			2		TX_fault		OK		
			3		Plugged		OK		
			4		Busy		OK		
			11-8		Buffer (full, empty, ...)		OK		
0x810	LC x status 0	ro	11-0	a	temp_sensor0	wf ===== Jim we need alarm limit and severity and ranges	OK		
			12		sendes clock used		OK		
			13		ok		OK		
			14		configured		OK		
			15		ladder_busy		OK		
0x811	LC x status 1	ro	11-0	a	temp_sensor1	warning	OK		
			12	b	crc error		OK		
			13		des bist pass		OK		
			14		des lock		OK		
			15		ladder_busy		OK		
0x812	LC x status 2	ro	11-0	a	temp_sensor2		OK		
			12		fib rx loss		OK		
			13		fib mod absent		OK		
			14		fib tx fault		OK		
			15		ladder_busy		OK		
0x813	LC x status 3	ro	11-0	a	temp_sensor3		OK		
			12		debuss oresent		OK		
			13		usb rdv_n		OK		
			14		usb present		OK		
			15		ladder_busy		OK		
0x814	LC x status 4	ro	11-0	l	nbr_hold		OK		
			12		hy_side		OK		
			13		hold		OK		
			14		test		OK		
			15		ladder_busy		OK		
0x815	LC x status 5	ro	11-0	l	nbr_test		OK		
			14-12	l*	serial bits 5-3		OK		
			15		ladder_busy		OK		
0x816	LC x status 6	ro	11-0	l	nbr_token		OK		
			14-12	l*	serial bits 2-0		OK		
			15		ladder_busy		OK		
0x817	LC x status 7	ro	11-0	l	nbr_abort		OK		
			14-12	l	Ladder #		OK		
			15		ladder_busy		OK		
0x818	LC x status 8	ro	15-0	m	ladder #	hybrid power status 15-0	OK		
Ladder card/Fiber 1									
0x900	LC FPGA confio control	rw	0				OK		To all 7 Fiber CHANNELS
Next ladder card Addr =0x100							OK		